Delta-sigma analog-to-analog converter solves tough design problems

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An analog-to-analog converter based on the ΔΣ modulator provides a creative and useful way to implement some common analog functions. Basic theory and several circuit examples show you how to apply the technique.

The use of delta-sigma (ΔΣ) ADCs and DACs, also known as sigma-delta and oversampling converters, has caught on in the last few years, particularly because of the DACs' application in CD players. However, a third converter category, ΔΣ analog-to-analog (A/A) converters, also exists. This concept, which actually involves an analog-to-digital-to-analog conversion, can be useful in the transmission of high-quality analog information through noisy environments, across isolation barriers, and through fiber-optic transmission systems. With slight modifications, this circuit can provide long audio delays and produce a high-efficiency, switching-type audio amplifier. Further potential applications include analog-in, analog-out, multiplierless, finite-impulse-response filters, ΔΣ-based switching power supplies, and ΔΣ-based communications-receiver demodulators.

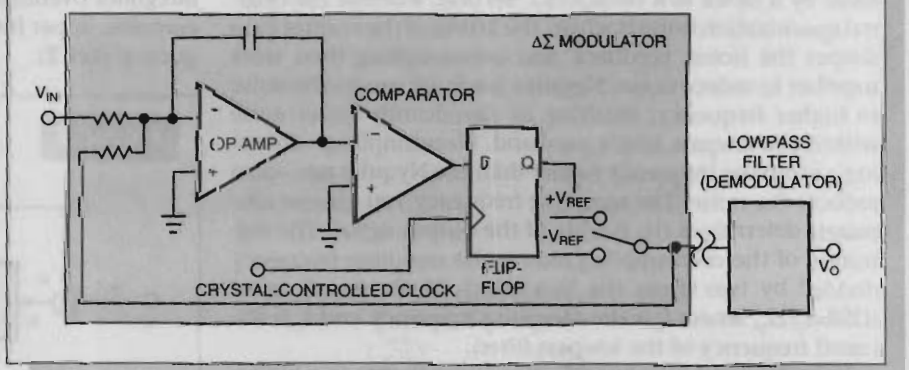
Fig 1 presents the basic ΔΣ A/A converter. The converter is essentially a ΔΣ-modulator block followed by an analog lowpass filter. You can also look at the converter as a 1-bit ADC followed by 1-bit DAC. The flip-flop output and lowpass filter comprise the final analog part of the analog-to-digital-to-analog conversion. The flip-flop produces a 1-bit conversion result that contains the original signal plus high-frequency noise. The actions of the modulator and oversampling work together to ultimately remove this noise.

The A/A converter closely resembles both ΔΣ DACs and ADCs, which both involve just minor modifications to Fig 1. For example, replacing the analog integrator with a digital accumulator implements a ΔΣ DAC. Changing only the lowpass filter in Fig 1 from an analog filter to a digital one creates a ΔΣ A/D converter. These digital, or decimation, filters cause an input-to-output latency, as does the analog filter in Fig 1. Consider the effect of this latency—essentially the delay of the lowpass filter—if you embed this converter in any feedback-control loop. **Ref 1** compiles significant papers on the subject of ΔΣ converters.

Analyzing the A/A converter

The ΔΣ A/A data converter in **Fig 1** looks much like a conventional control loop and is easiest to analyze using traditional feedback methods. To perform the analysis, you must linearize some elements in the circuit. To create a linear model, treat the digital elements—comparator and flip-flop—as simply the summation of the desired signal, e_i, and a white-noise element, e_n (**Fig 2a**). Thus, the 1-bit quantizer

FIGURE 1



The ΔΣ A/A converter is essentially a ΔΣ-modulator block followed by an analog lowpass filter. You can also look at the circuit as a 1-bit ADC followed by a 1-bit DAC.

is analytically similar to high-resolution quantizers because it produces the desired signal plus an undesired noise component (**Fig 2b**). The resulting quantization noise for the 1-bit quantizer is typically higher than the signal itself, but the model nevertheless provides good results. **Fig 3** is a block diagram of the ΔΣ A/A converter with the linearized output.

The loop equations for this system show how the ΔΣ circuit reduces the huge quantization noise that the 1-bit quantizer produces to an acceptable level. If the integrator gain equals K/s, then the loop equations become

$$x = v_i - y,$$

and

$$y = e_n + \frac{K}{s}x = e_n + \frac{K}{s}(v_i - y),$$

which results in

$$y(s+k) = se_n + Kv_i.$$

Treating the response, y, to the signal and noise independently gives

$$y_n = \frac{s}{s+K}e_n \quad (\text{for } v_i = 0),$$

and

$$y_s = \frac{K}{s+K}v_i \,(\text{for } e_n = 0).$$

If you choose the break frequency, ω_0, of the lowpass filter in **Fig 3** such that ω_0 is much less than K but includes all input signals of interest, then the respective noise and signal outputs of the ΔΣ circuit are

$$v_{on} \approx \frac{s}{K}e_n \,(\text{for } v_i = 0), \qquad (1)$$

and

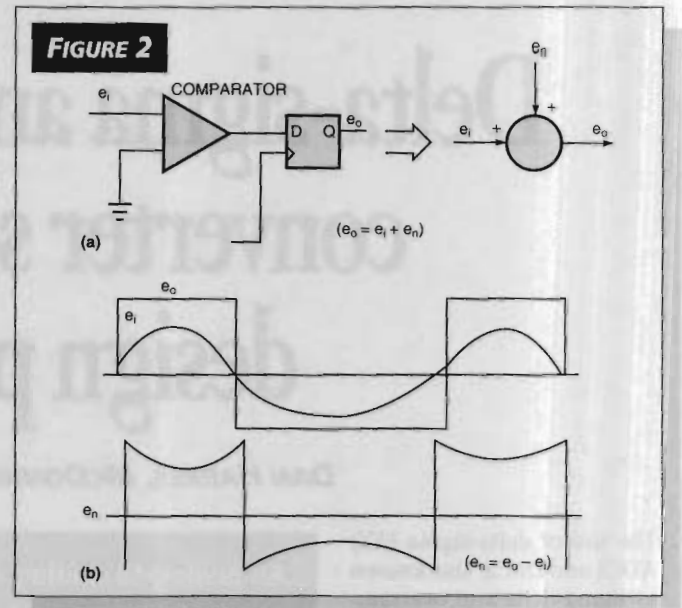
$$v_{os} \approx v_i \,(\text{for } e_n = 0). \qquad (2)$$

Eqs 1 and **2** indicate that such a first-order (single-integrator) circuit can pass the input signal without attenuation while differentiating—and, therefore, dramatically reducing—the quantization noise. This point has important implications for the performance of a ΔΣ A/A converter. First, this converter reduces the noise at any frequency within the passband by a factor ω/K ($\omega \le \omega_0 << K$). Second, whereas the original quantization noise is white, the action of the control loop shapes the noise. Feedback and oversampling then work together to reduce noise. Negative feedback moves the noise to higher frequency, resulting in significantly lower noise within the lowpass filter's passband. Oversampling—choosing a sampling frequency higher than the Nyquist rate—also reduces the noise. The sampling frequency you choose ultimately determines the fidelity of the output signal. The definition of the oversampling ratio is the sampling frequency divided by two times the bandwidth of the input signal ($OSR = f_s/2f_0$, where f_s is the sampling frequency and f_0 is the cutoff frequency of the lowpass filter).

To understand how quantization noise moves to a higher frequency, consider what happens when the input is a dc level halfway between the maximum and minimum modulator-output levels. For **Fig 1**, this point corresponds to a 0V input because the modulator has output levels equal to $\pm V_{REF}$. In this case, the flip-flop alternately selects between these two voltages, producing the original dc level of 0V plus a square wave that constitutes the noise. The noise of a properly designed converter is high in amplitude, but the fundamental frequency of the noise spectrum is considerably higher than the lowpass filter's cutoff frequency of f_0. Thus, although the converter transmits the 0V signal intact, the converter quite heavily attenuates the quantization noise. This noise attenuation is possible because the noise has increased to a relatively high frequency.

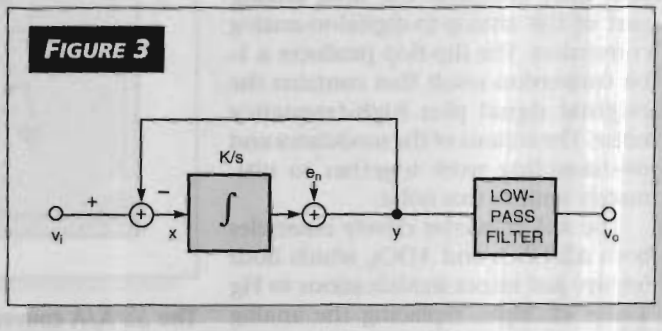
Eq 1 shows the significance of the loop gain, K, in reducing the noise within the modulator's passband. From a noise-minimization point of view, make K as large as possible. However, other considerations, such as loop stability and integrator overload, impose limits on the magnitude of K. A common upper limit for K is $K=f_s$, where f_s is the sample frequency (**Ref 2**).

FIGURE 2



To analyze the A/A converter as a linear system, you can treat the comparator and flip-flop as simply the summation of the desired signal, e_i, and a white-noise element, e_n (a). Thus, the 1-bit quantizer produces the desired signal plus some undesired noise component (b).

FIGURE 3



This block diagram of the ΔΣ A/A converter incorporates the linearized versions of the comparator and flip-flop.

The first-order ΔΣ converter is the simplest case. This order might also be the best choice for applications in which you can trade off performance for circuit simplicity. However, higher order converters incorporating two or more integrators in the loop provide lower noise for a given value of oversampling ratio.

The second-order loop in **Fig 4** replaces the integrator constants of **Fig 1** with the actual resistors and capacitors that create those integrator constants. Just as with **Fig 1**, you can analyze this circuit by replacing the comparator and flip-flop with the linear summer plus quantization noise source. Linearizing the analog/digital interface of this circuit and treating the resulting circuit as a conventional control loop results in the signal-transfer function of

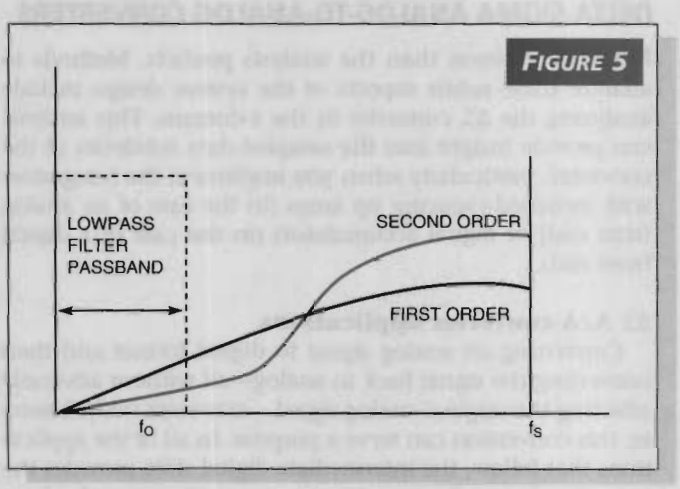
$$y_s = \frac{1}{R_2R_4C_1C_2} \cdot \frac{1}{s^2 + s\frac{1}{R_3C_2} + \frac{1}{R_1R_2C_1C_2}} v_i, \ (e_n = 0),$$

and noise-transfer function of

$$y_n = \frac{s^2}{s^2 + s\frac{1}{R_3C_2} + \frac{1}{R_1R_2C_1C_2}} e_n, \ (v_1 = 0),$$

A good choice for these resistors and capacitors would likely be $R_1=R_2=R_4=R$, $C_1=C_2=C$, and $R_3=0.7R$, resulting in a critically damped system.

Fig 5 compares the noise-transfer functions of first- and second-order loops. As the curves indicate, the passband noise of the second-order loop is significantly lower than that of the first-order loop. Also, theory predicts that for each doubling of the f_S, the S/N ratio of the first-order ΔΣ converter increases by 9 dB and that of the second-order converter increases by 15 dB. In general, the S/N ratio of the ΔΣ converter increases by 3 dB · (2L+1) for every doubling of f_S, where L is the order of the ΔΣ converter (**Ref 1**). This point implies that, given a sufficient number of integrators in the loop, you can reduce the noise in a ΔΣ converter to any desired level. In practice, however, loops of order greater than two tend to be unstable. Techniques to stabilize higher order loops do exist (**Refs 3** and **4**), but the second-order converter generally provides the highest performance for any straightforward approach.



These noise-transfer functions of first- and second-order loops show that the passband noise of the second-order loop is significantly lower than the noise of the first-order loop.

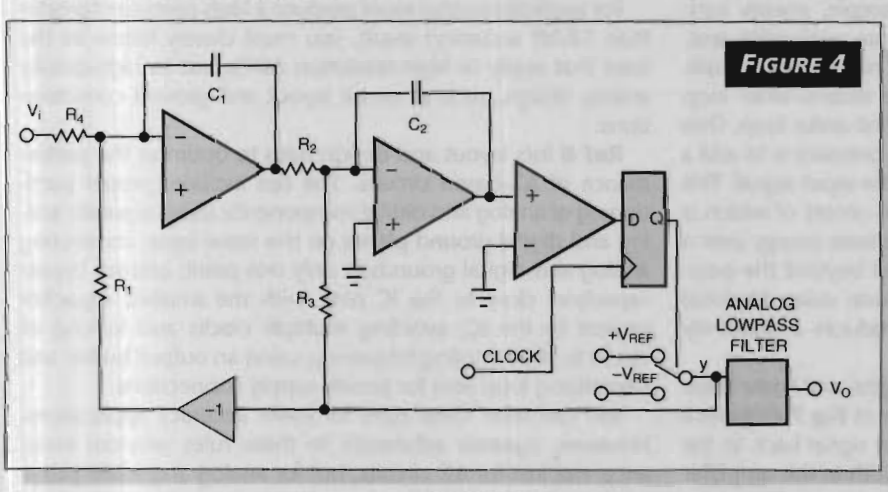
Higher order loops randomize the quantization noise, a desirable effect that is due to the interaction of the multiple integrators. This greatly reduces a common problem of first-order ΔΣ converters, in which the noise takes the form of a standing sequence of ones and zeros. The resultant "tones" within the passband are more noticeable than a comparable amount of energy in a random quantization sequence.

The model has limitations

Although this analysis provides insight, it also ignores certain system aspects because of the act of approximating the sampled-data and nonlinear elements with linear, continuous-time models. For example, although the noise performance of any ΔΣ converter improves with sampling frequency, the simple analytical approach can only indirectly show this fact by equating loop gain with sample frequency.

Additionally, the preceding analysis implies that the comparator has infinite gain and zero response time. In practice, both comparator gain and response time are limited. In the isolation-amplifier example that follows, a CMOS gate, which has a gain of only about 100, serves as comparator. Consequently, the comparator can spend a good deal of time in its linear region while transitioning between states, aggravating problems, such as stability, that relate to response time. Conventional comparators likely have higher gains but may have longer response times. The linearized model provides no insight into how these limitations affect performance.

The analysis assumes that the quantization noise is uncorrelated with the signal. At low frequencies, however, there is some correlation, and noise per-



This second-order ΔΣ A/A converter replaces the integrator constants of Fig 1 with the resistors and capacitors that create those constants.

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formance is worse than the analysis predicts. Methods to analyze these subtle aspects of the system design include analyzing the ΔΣ converter in the z-domain. This analysis can provide insight into the sampled-data subtleties of the converter, particularly when you implement the integrators with switched-capacitor op amps (in the case of an analog front end) or digital accumulators (in the case of a digital front end).

ΔΣ A/A-converter applications

Converting an analog signal to digital format and then converting the signal back to analog—all without adversely affecting the original analog signal—may seem odd. However, this conversion can serve a purpose. In all of the applications that follow, the intermediate digital state provides the opportunity to solve a problem in a unique way and, often, in better ways than conventional methods. These circuits have their pitfalls and, like other analog circuits, require good layout and grounding techniques. (See **box**, "How to avoid ΔΣ-converter pitfalls.")

One design challenge is the robust transmission of high-fidelity analog signals over twisted-pair cable. Transmitting these signals over relatively long distances (a few feet to a few thousand feet) without sacrificing precision is the main problem. Differential transmission over shielded twisted-pair wire reduces the susceptibility of these signals to EMI compared to single-ended transmission. However, EMI may still pose a problem, particularly in the presence of adjacent, rapidly switching voltages. Even in quiet environments, other problems can seriously degrade the signal, such as phase distortion resulting from transmission-line reactance.

As a general rule, noise performance suffers with direct analog transmission, as any user of 1960s-vintage long-distance phone service can attest. In addition to the noise, tight gain tolerance over long lines is difficult to achieve because of the inability to precisely control transmission-line attenuation.

One solution to this problem is to convert the analog signal using a conventional ADC, send the digital data over the twisted pair, and then convert the digital data back to analog form using a conventional DAC. This approach is the

HOW TO AVOID ΔΣ-CONVERTER PITFALLS

Designing with a ΔΣ A/A converter involves three potentially serious problems:

- A susceptibility to power-supply noise. This problem arises because the output of the ΔΣ modulator is a switch that ideally connects the +V, –V, or ground directly to the load. Although the ΔΣ modulator's negative feedback somewhat attenuates the noise at low frequencies, the feedback likely has little gain at the modulator's clock frequency. Interference at higher frequencies, particularly at multiples of the sampling frequency, mixes down and likely hurts the design's performance.
- "Tones" that can arise spontaneously or as a function of input voltage. Small spikes may appear in the output spectrum of a ΔΣ circuit. These spikes, which are undesirable in many applications, rise above the noise floor within the passband of the circuit. In audio applications, for example, energy concentrated at just a few frequencies is more noticeable and, therefore, more objectionable than white noise whose amplitude is spread over the audio band. The second-order loop exhibits fewer of these artifacts than the first-order loop. One fairly straightforward way of reducing this behavior is to add a small dither signal (a random voltage) to the input signal. This seemingly odd addition of random signal—most of which is outside the loop's passband—spreads the tone energy over a range of frequencies, including those well beyond the passband. Ways to produce such noise include using National Semiconductor's MM5437 IC, which produces a uniformly distributed random-noise output.
- Instability and distortion from slow digital and linear-feedback components. The ΔΣ audio amplifier of **Fig 7** includes a differential amplifier that feeds the output signal back to the ΔΣ input. Low slew rate and gain bandwidth in this amplifier cause poor replication of the output waveform with consequent harmonic distortion and higher noise levels. Amplifiers that feed back the modulator output should have a bandwidth considerably greater than that of the loop bandwidth. The integrator op amps should likewise have a higher gain bandwidth than does the integrator constant, so that the op amps do not interact with and, thereby, reduce the integrator constant. Some systems split the output signal, feeding one version back to the ΔΣ input and sending the other through a medium, such as a data link. In these systems, the receiver must reclock and rereference the digital-modulation signal to avoid timing or gain mismatches that could seriously affect performance. The isolation amplifier of **Fig 9** demonstrates such a re-establishment of clocking and reference.

Circuit layout is critical

For applications that must produce a high-precision (greater than 12-bit accuracy) result, you must closely follow all the rules that apply to high-resolution ADCs and to high-quality analog design, such as circuit layout and ground considerations.

Ref 8 lists layout and design rules to optimize the performance of ΔΣ-based circuits. The tips include: proper partitioning of analog and digital components; using separate analog and digital ground planes on the same layer; connecting analog and digital grounds at only one point; placing bypass capacitors close to the IC pins, with the smallest capacitor nearest to the IC; avoiding multiple clocks and locking all clocks to the sampling frequency; using an output buffer; and minimizing loop area for power-supply connections.

You can relax these rules for lower accuracy applications. However, rigorous adherence to these rules provides insurance, not just for ΔΣ circuits, but for analog and analog/digital designs.

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solution that telephone companies employ and the best choice for some applications. However this scheme requires additional circuit requirements. For example, a sharp antialiasing filter and an S/H amplifier must precede the ADC, and a parallel-to-serial converter may be necessary at the ADC's output. In addition, the DAC's input may require parallel data, necessitating a serial-to-parallel conversion, and the DAC may require a deglitching S/H amplifier and an interpolation filter. Circuit complexity increases as accuracy requirements increase. An alternative way of achieving this analog-to-digital-to-analog process would be useful.

Digital transmission using ΔΣ A/D/A

The converter approach in **Fig 6** circumvents the problems of direct analog transmission and keeps the circuitry fairly simple. The circuit requires few ICs, and IC manufacturers are now beginning to produce ΔΣ modulator ICs, such as the Texas Instruments 58A20, which further decrease circuit complexity. In addition, you can generally keep the distortion low because the ΔΣ circuit uses only two voltage levels, thereby eliminating the distortion associated with conventional multilevel ADCs and DACs.

The converter in **Fig 6** achieves gain stability with a reference at both the transmitter and receiver ends. The circuit reduces the gain error to the difference between the two references, which is generally small. You must control the phase relationship of the transmit and receive clocks in **Fig 6**, so that the receiver samples the data at the correct point. One way to achieve this synchronization is simply to ship the transmit clock down a second twisted pair. The isolation-amplifier design in **Fig 8** takes this approach.

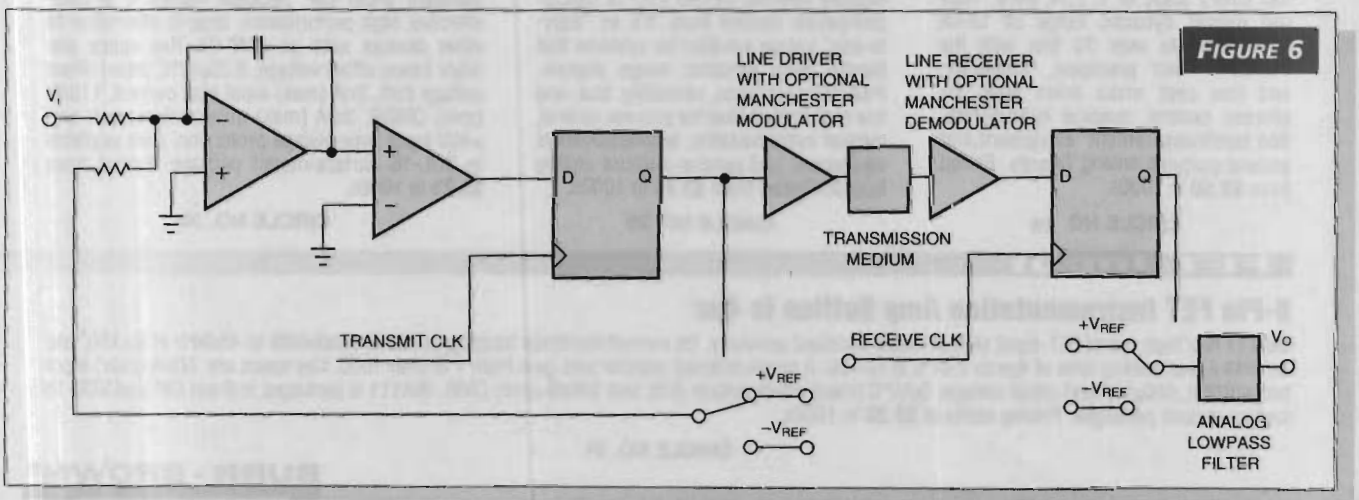
Alternatively, you can eliminate the second transmission line by combining data and clock on the same twisted pair. You can use Manchester encoding for the data at the transmitting end and Manchester decoding for the data at the receiving end. Manchester encoding offers a transition in the middle of each bit, guaranteeing good clock recovery; no dc component in the transmission spectrum, allowing ac-coupled transmission; and, for this application, a transmission spectrum predominantly at frequencies well above the passband of the converter, minimizing noise interference for the sensitive linear circuits.

Fiber-optic transmission provides noise immunity, enormous potential bandwidth, small size and weight, and electrical isolation. You can send analog signals across optical fibers in analog form via "intensity modulation," in which the optical source intensity is directly proportional to signal amplitude. However, with this technique the fiber-optic system generally displays an S/N ratio at least 40 dB lower than that of an electrical transmission system. This drawback makes intensity modulation unsuitable for high-fidelity analog transmission (**Ref 5**).

A better choice in such situations is a system similar to the electrical-transmission system. First, convert the signal to a digital-transmission stream using the ΔΣ A/A converter and optionally combining data and clock with Manchester encoding. As with the electrical-transmission system, this system offers tight gain stability, high S/N ratio, and low distortion because only two digital states exist at the output.

The ΔΣ A/A converter can also create analog delays. Although several clocked analog-delay ICs are available, they generally have a maximum S/N ratio of around 60 dB, which is insufficient for some applications, such as high-fidelity audio. The A/A-converter alternative involves replacing the flip-flops and transmission components in **Fig 6** with a serial shift register. With the high-density memories available today, it becomes feasible to delay high-fidelity audio signals up to several seconds.

The ΔΣ A/A converter also suits audio applications, including echo and ambiance effects, public-address systems, and speech-correction devices. The design in **Fig 7**, a block diagram of an A/A-converter-based power audio amplifier, uses a second-order loop like the one in **Fig 4**. For most such amplifiers, the output of the modulator is a voltage, ±V, that is considerably higher than the voltages that power the integrators and other components of the ΔΣ circuit. For **Fig 7**'s



Using the ΔΣ A/A converter to implement direct digital transmission across twisted-pair cable circumvents the problems of direct analog transmission and keeps the circuitry fairly simple.

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100W amplifier, this output voltage would be around ±45V. Consequently, the linearized model to analyze this circuit would include a gain block, G, after the comparator, to account for signal gain. For proper analysis, the block diagram would also include a 1/G attenuation block to normalize the loop gain. In practical implementations, this attenuation stage would likely comprise resistor dividers to ensure voltages input to any subsequent feedback op amps would be within acceptable input ranges.

A good output for this design is an H-bridge, which requires only a positive supply voltage to generate a bipolar swing across the load. Besides requiring only one supply, this approach should ease EMI problems because the current flowing through the supply wires is virtually constant, regardless of output state. A ground-referenced load is also an option.

The demodulator for **Fig 7**'s converter is an LC network that terminates in an 8Ω loudspeaker. The idea of using a loudspeaker as a filter-termination resistance is not new; passive crossover networks generally use loudspeaker drivers in this way. However, the situation in **Fig 7** is less clear-cut than that of crossovers. The termination impedance in the **figure** might comprise a collection of speaker drivers and their associated crossovers (that is, a loudspeaker assembly), rather than a single speaker driver. Instead of the ideal 8Ω resistance, a typical loudspeaker has a more complex impedance. However, this less-than-ideal impedance should cause no problem for the following reasons:

- Within the audio passband, the noise of the A/A converter is low by virtue of the ΔΣ design. The circuit doesn't rely on the LC filter attenuation to do anything except pass an undistorted signal.
- Filtering is necessary beyond the audio passband to attenuate the large quantization effects of ΔΣ modulation. However, the purpose of this filtering is primarily to protect the loudspeakers. The human-hearing response falls sharply after a few kilohertz, creating a natural filtering response for listeners and making high-frequency imperfections less problematic (**Ref 6**).
- You can set the break frequency of the demodulating filter to around 25 kHz, which is somewhat beyond the audio passband. This approach puts most interactions between the demodulation filter and other reactionary elements outside the audio passband.

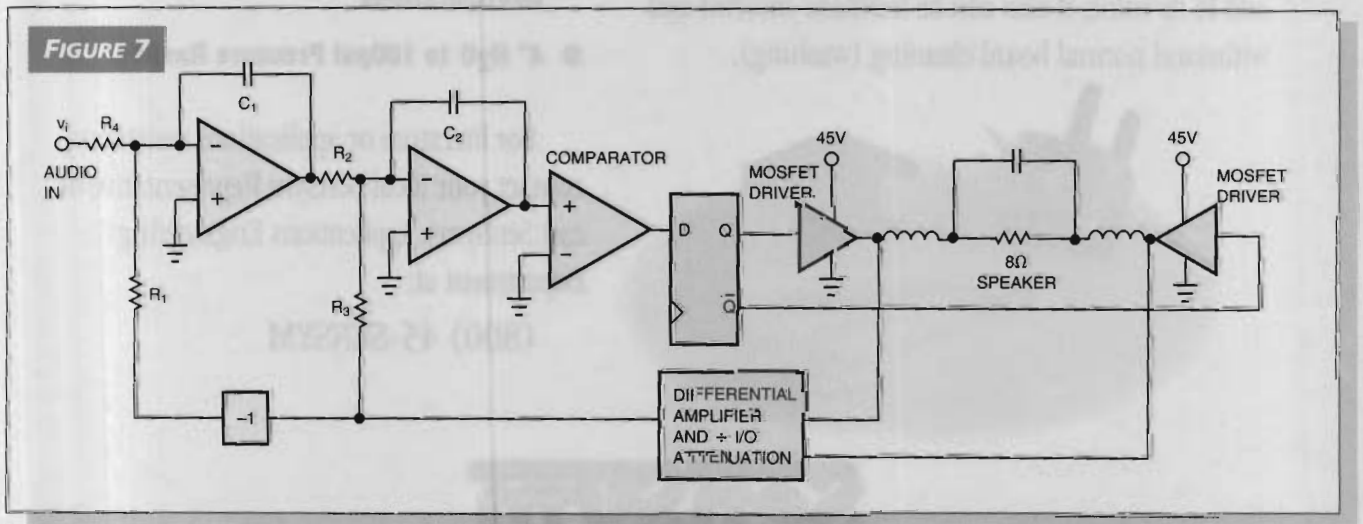
Transmitting across an isolation barrier

Another tough-to-solve design problem is transmitting a relatively high-fidelity analog signal across an isolation barrier. Isolation barriers are typically necessary in systems that must measure low-level signals in the presence of a high common-mode voltage, in systems in which ground loops might otherwise occur, and in systems that provide patient-safe interfaces.

Such applications sometimes use intensity-modulated linear optocouplers, which are similar to the intensity-modulated analog fiber-optic links. However, such linear optocouplers generally have relatively high distortion and poor gain stability. Other analog techniques, such as transmitting the analog signal through transformers or capacitors, may pose problems. These techniques may be unable to handle a sufficiently large range of frequencies, and neither the transformer nor the capacitors accommodate dc signals. Off-the-shelf isolation amplifiers employ various methods for achieving isolation, but these amplifiers' performance may be insufficient for your application. You also may be unable to use these amplifiers in systems operating in harsh environments and systems requiring use of a customer's approved parts list.

The ΔΣ A/A converter provides a simple means of achieving isolation and design flexibility. For example, the space application of **Fig 8**'s isolation amplifier precludes the use of most low-power comparators because of their susceptibility to radiation damage in orbit (**Ref 7**). CMOS logic gates substitute for the comparators with no change in performance.

Fig 8 is similar to **Fig 1**, except that the clock input, ΔΣ output, and power-supply input are all electrically isolated from any external circuits. **Fig 9**, a schematic of the design of the



This A/A-converter-based power audio amplifier uses a second-order loop.

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spacecraft circuit, measures a dc voltage of a solar array isolated from the spacecraft ground. The modulator of **Fig 9a** runs from a single power-supply voltage that comes in as a square wave at 20 kHz (POWER+ and POWER–), which the circuit then rectifies to produce the main supply voltage of 12V. In this circuit, the sampling frequency equals the clock input divided by 2. The power and clock signals have the same source, thus satisfying one of the rules in the **box** "How to avoid ΔΣ-converter pitfalls."

A REF-05, IC_5, regulates the 12V supply down to a precise 5V. The resulting signal, 5Vm, where "m" stands for modulator, powers the logic elements including the flip-flop that provides the unipolar feedback signal. The design minimizes all current demands from this 5V source to minimize modulation of the reference feedback voltage. The circuit also creates a precise 2.5V (5Vm/2) by summing both outputs of the 50% duty cycle, producing the IC_{4A} flip-flop. The 2.5V reference provides for single-supply operation of the ΔΣ circuit, which maintains power-supply simplicity. You could use a resistor divider to divide 5Vm by 2, but the result would have an error equal to the sum of the errors that each resistor contributes. Thus, the conventional approach requires precision resistors. Assuming that the on-resistance of the 54HC74 is negligible compared to that of the 100-kΩ summing resistors, the summation of the square-wave output of the 5Vm-powered IC_{4A} produces a summing node voltage of

$$v_{C1} = \frac{1}{2}\frac{R_6}{R_6+R_7}5v_m + \frac{1}{2}\frac{R_7}{R_6+R_7}5v_m + \frac{1}{2}5v_m, \quad (3)$$

where v_{C1} is C_1's average voltage.

The resulting voltage is independent of the tolerances of R_6 and R_7. Actually, **Eq 3** applies only to the average values and, therefore, predicts only dc performance. Any mismatch between R_6 and R_7 creates a small residual ac voltage, but C_1 attenuates this voltage. This voltage also should not affect performance because the voltage occurs synchronously with the sample clock and has an average value of zero over each sample period (see **box**). **Fig 9a**'s resulting circuit takes a 0 to 160V-dc input voltage, divides it, and compares it to the flip-flop's output. The circuit scales the resistors, so that a 0V-dc input corresponds to a constant flip-flop output of 5Vm and a 160V-dc input corresponds to a constant flip-flop output of 0V.

Fig 10 shows the components that determine proper scaling of the input. The parallel combination of R_2 and R_3 in series with R_1 divides the large incoming voltage. Also, in the case of any momentary lapses of power on IC_{1A}'s op amp, R_2 and R_3 prevent high voltages at the op-amp input.

To minimize offset current, the input resistance at IC_{1A}'s inverting input should equal 50 kΩ because that is the resistance at the noninverting input. Thus,

$$R^- = (R_4+R_5)\left\|\left[(R_3+R_2)\|R_1\right]\right. = R^+ = 50\Omega, \quad (4)$$

where R^- and R^+ are the inverting and noninverting resistances, respectively. The equations for the two input currents for IC_{1A} are as follows:

$$i_1 = \frac{v_o - 2.5}{R_4+R_5},$$

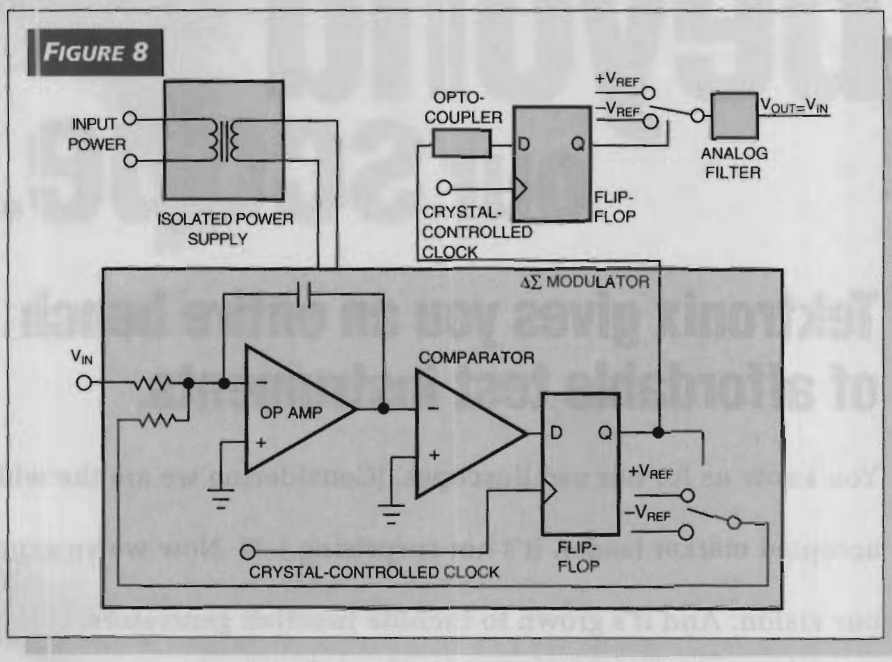
$$i_2 = \frac{v_m - 2.5}{R_3},$$

where v_o is IC_{4B}'s average output and

$$v_m = \frac{R_2\|R_3}{R_1+R_2\|R_3}v_i + \frac{R_1\|R_3}{R_3+R_1\|R_2}2.5. \quad (5)$$

The boundary requirements are that 0 and 160V-dc input voltages correspond to respective 5 and 0V-dc output voltages. Inserting those requirements along with the condition of **Eq 4** into **Eq 5** lets you solve for the following values: R_1=250 kΩ, R_2=8.064 kΩ, R_3=93.1 kΩ, R_4=100 kΩ, and R_5=1 kΩ.

FIGURE 8

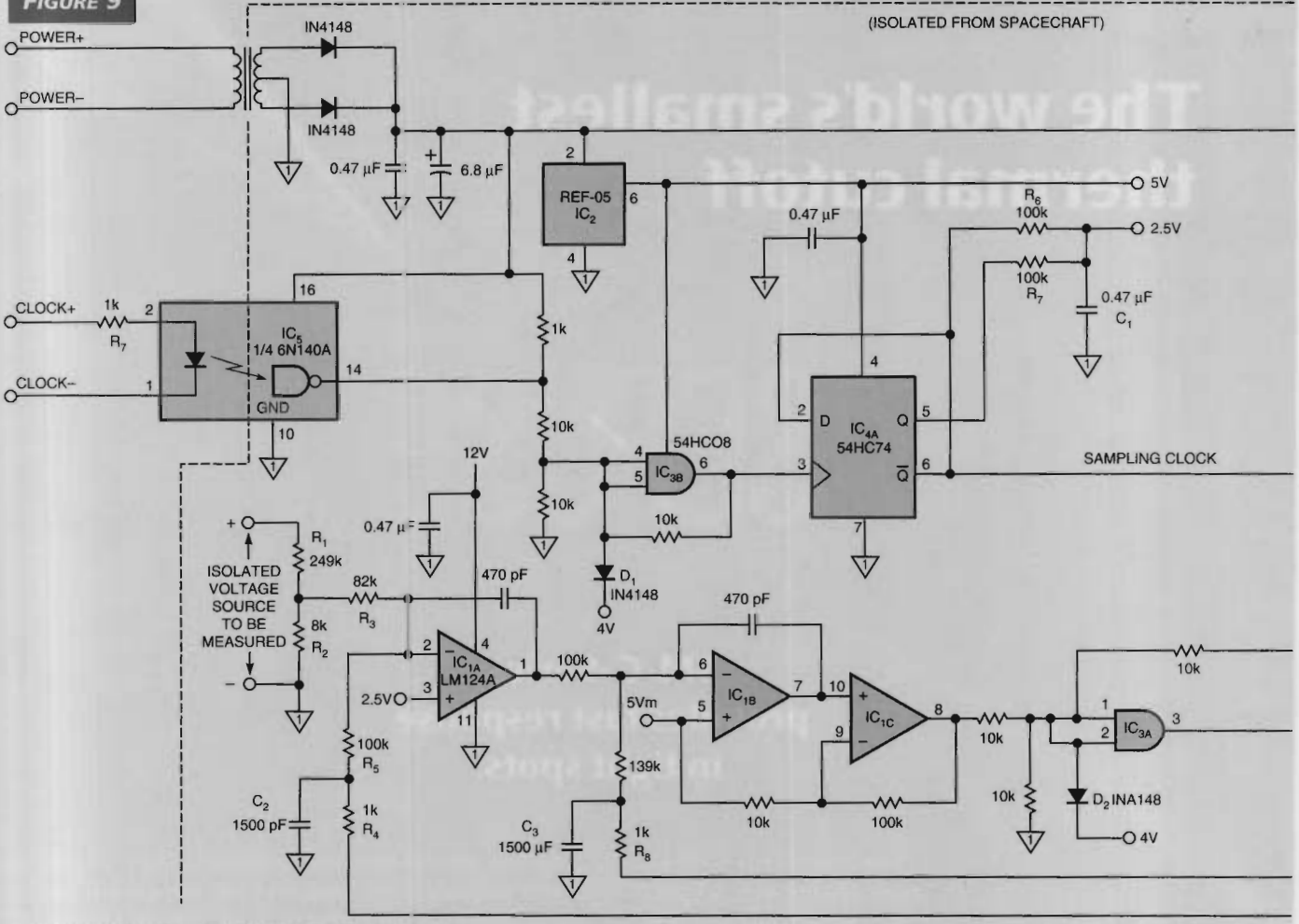


This isolation-amplifier block diagram is similar to that in Fig 1, except that the clock input, ΔΣ output, and power-supply input are all electrically isolated from any external circuits.

Making an AND gate into a comparator

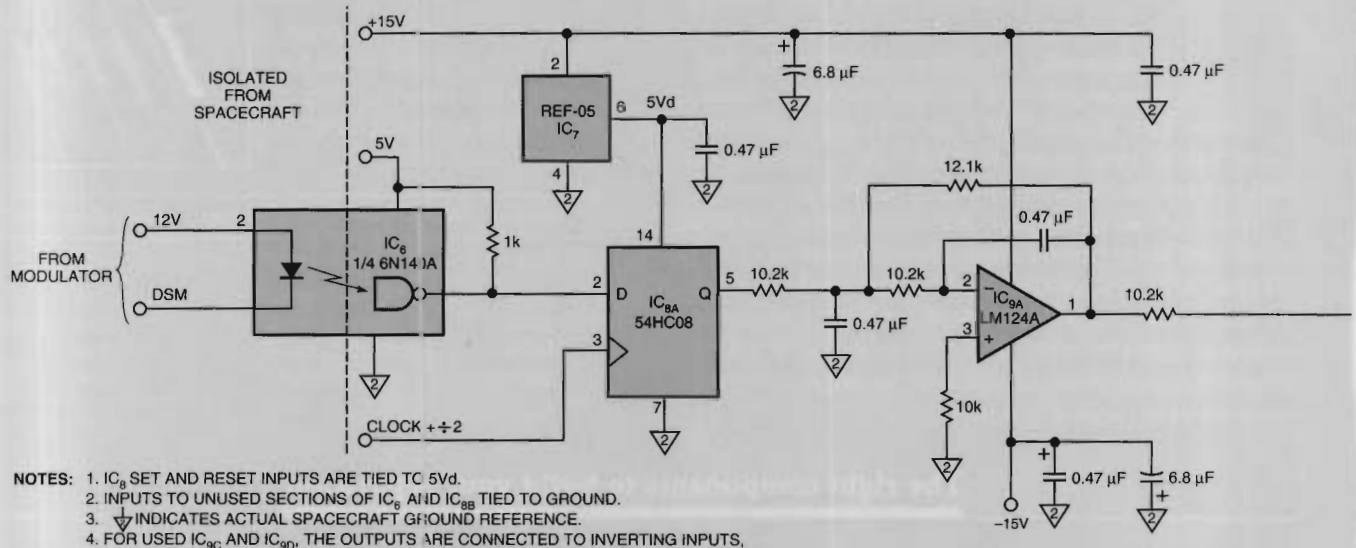
Because most low-power comparators degrade at high radiation levels and because the radiation-tolerant comparators for this project consumed too much power, **Fig 9a** uses a CMOS 54HC08 AND gate, IC_{3B}, as a comparator. This choice may seem strange, but a gate is just a comparator with a fixed threshold. (For simplicity, consider only single-input devices.) The dc threshold setting is imprecise, so the application must be able to tolerate a 20% or so variation in this setting.

FIGURE 9



NOTES: 1. IC_4 SET AND RESET INPUTS ARE TIED TO 5Vm.
2. INPUTS TO UNUSED SECTIONS OF IC_5 AND IC_{3d} CONNECTED TO ⏚
3. ⏚ INDICATES ISOLATED REFERENCE.

(a)



NOTES: 1. IC_8 SET AND RESET INPUTS ARE TIED TO 5Vd.
2. INPUTS TO UNUSED SECTIONS OF IC_6 AND IC_{8B} TIED TO GROUND.
3. ⏚ INDICATES ACTUAL SPACECRAFT GROUND REFERENCE.
4. FOR USED IC_{9C} AND IC_{9D}, THE OUTPUTS ARE CONNECTED TO INVERTING INPUTS, AND THE NONINVERTING INPUTS ARE TIED TO ⏚.

(b)

This spacecraft circuit measures a dc voltage of a solar array, which is isolated from the spacecraft ground. The circuit in (a) is the modulator portion; (b) is the demodulator.

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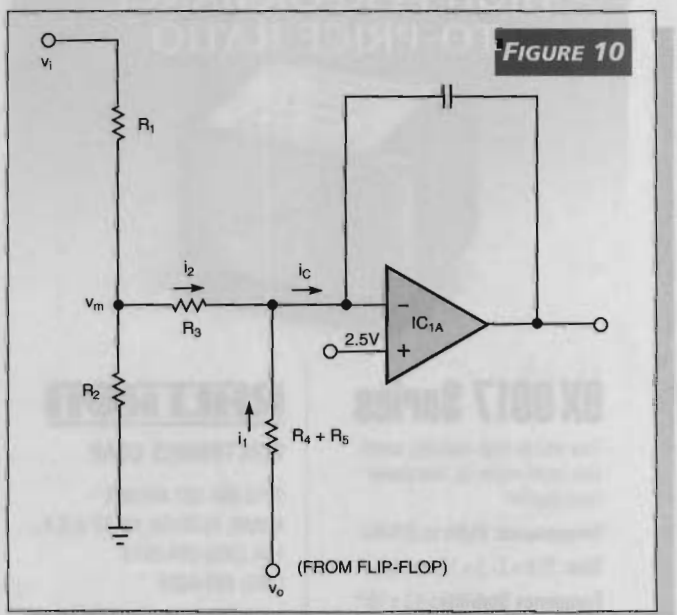
The ΔΣ A/A converter is such an application. Because the comparator follows the integrators, the control loop divides any offset voltage by the value of the converter's open-loop gain. Thus, any comparator offset voltage is virtually insignificant at any frequency within the passband. The only stability requirement for such thresholds is that the voltage remain stable, that is, have minimal jitter, over short periods. Consequently, the CMOS gate works well as a comparator.

Noise is also an important consideration. Recall that these gates generally have gains of around 100. For inputs that change slowly compared to the gate response, the gate input can remain near its threshold for a long time. This situation could cause the output to chatter between states, creating excessive noise. The gate input's remaining near its threshold for a long time could also cause the gate to behave like a linear amplifier, consuming excessive power and heating up. To avoid this situation, the circuit adds a considerable amount of hysteresis and another gain stage (IC_{1C}) preceding the gate. Such comparator hysteresis generally increases the quantization noise in the passband. However, in this case, the oversampling ratio is so high (>200) that the additional noise is insignificant.

Finally, D_1 and D_2 provide 4.7V clamps, which, with the 4V source of IC_{1D}, protect the CMOS gates from overvoltage. Because the gates' thresholds are nominally 2.5V, this clamp voltage does not affect their operation. **Fig 9a** inverts the feedback signal (the gain block of –1 in **Fig 7**) by simply using the inverted logical output of IC_{4B}. The R_4/C_2 and R_8/C_3 networks filter these feedback signals, limiting them to about 100 kHz. This signal is an order of magnitude above the sampling frequency but an order of magnitude below the LM124A's gain bandwidth. This technique avoids overload



R_1, R_2, and R_3 provide the proper input scaling for IC_{1A}'s input. In the case of any momentary lapses of power, R_2 and R_3 also prevent high voltages at the op-amp input.

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to the op-amp input stage.

In **Fig 9b**, a 6N140A optocoupler, IC_6, transmits the ΔΣ A/A converter's output across the isolation barrier. You need not transmit the clock across the isolation barrier because the clock already exists on the nonisolated side of the barrier. The circuit uses IC_{8A} to reclock the recovered signal and IC_7 to re-establish the gain. A fourth-order, 30-Hz filter with gain of 2, which comprises IC_{9A} and IC_{9B}, provides the demodulation.

The overall isolation amplifier performed well. The dc characteristics of the op amps and resistors determine dc accuracy. Residual rms noise in the output was less than 0.02% of full scale for 10 to 150V input voltages, rising to about 0.3% at the extremes of the input range. This error increase at input-range extremes is typical of ΔΣ amplifiers, and you generally design such amplifiers with a little "head room" at the extremes to avoid using those regions. EDN

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Author's biography

Dan Harres is a principal technical specialist at McDonnell Douglas Aerospace in St Louis where he has worked for 20 years. He has developed flight-simulator visual displays, space-based optical communications systems, and spacecraft instrumentation. Dan holds a bachelor's degree in computer engineering from the University of Illinois and a master's in electrical engineering from the University of Missouri. He is currently a doctoral student at Washington University in St Louis.